WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a memory cell array having a plurality of non-volatile memory cells each having three or more threshold voltage levels;

word lines, bit lines and source lines connected to said memory cells;

a row decoder configured to select one of said word lines; and

a column decoder configured to select one of said bit lines,

wherein when said three threshold voltage levels are given by Vt1, Vt2 and Vt3 (Vt1<Vt2<Vt3), respectively, the following steps (1) to (5) are executed to carry out a program operation,

(1) loading program data,

(2) programming for said memory cells to be given by the threshold voltage Vt2 being accomplished by a first gate voltage,

(3) detecting whether said memory cells have the threshold voltage Vt2, and carrying out said step (2) using a second gate voltage higher than said first gate voltage when said memory cells do not have the threshold voltage Vt2, followed by a next step (4) when said memory cells have the threshold voltage Vt2,

(4) programming for said memory cells to be given by the threshold voltage Vt3 being carried out by a third gate voltage having a value equal to or higher than a maximum value of a program gate voltage of said memory cells to be given by the threshold voltage Vt2, and

(5) detecting whether said memory cells have the threshold voltage Vt3, and re-executing said step (4) when said memory cells do not have the threshold voltage Vt3, and finishing said program operation when said memory cells have the threshold voltage Vt3.

2. A non-volatile semiconductor memory device comprising:

a memory cell array having a plurality of non-volatile memory cells each having three or more threshold voltage levels;

word lines, bit lines and source lines connected to said memory cells;

a row decoder configured to select one of said word lines; and

a column decoder configured to select one of said bit lines,

wherein when said three threshold voltage levels are given by Vt1, Vt2 and Vt3 (Vt1<Vt2<Vt3), respectively, the following steps (1) to (5) are executed to carry out a program operation,

(1) loading program data,

(2) programming for said memory cells to be given by the threshold voltage Vt3 being accomplished by a voltage value equal to or higher than a maximum value of a program gate voltage of said memory cells to be given by the threshold voltage Vt2,

(3) detecting whether said memory cells have the threshold voltage Vt3, and re-executing said step (2) when said memory cells do not have the threshold voltage Vt2, followed by a next step (4) when said memory cells have the threshold voltage Vt2,

(4) programming for said memory cells to be given by the threshold voltage Vt2 being carried out by a first gate voltage, and

(5) detecting whether said memory cells have the threshold voltage Vt2, and executing said step(4) using a second gate voltage higher than said first gate voltage when said memory cells do not have the threshold voltage Vt2, while finishing said program operation when said memory cells have the threshold voltage Vt2.

3. A non-volatile semiconductor memory device comprising:

a memory cell array having a plurality of non-volatile memory cells each having four or more threshold voltage levels;

word lines, bit lines and source lines connected to said memory cells;

a row decoder configured to select one of said word lines; and

a column decoder configured to select one of said bit lines,

wherein when said four threshold voltage levels are given by Vt1, Vt2, Vt3 and Vt4 (Vt1<Vt2<Vt3<Vt4), respectively, the following steps (1) to (5) are executed to carry out a program operation,

(1) loading program data,

(2) programs for said memory cells to be given by the threshold voltage Vt2 and for said memory cells to be given by the threshold voltage Vt3 being accomplished by a first gate voltage,

(3) detecting whether the threshold voltages of said memory cells have Vt2 and Vt3, respectively, and re-executing said step (2) when said memory cells do not have the threshold

voltages Vt2 and Vt3, followed by a next step (4) when said memory cells have the threshold voltages Vt2 and Vt3,

(4) programming for said memory cells to be given by the threshold voltage Vt4 being carried out by a voltage value equal to or higher than a maximum value of a program gate voltage of said memory cells to be given by one of Vt2 and Vt3, and

(5) detecting whether said memory cells given by Vt4 have the threshold voltage of Vt4, and re-executing said step (4) when said memory cells do not have the threshold voltage Vt4, while finishing said program operation when said memory cells have the threshold voltage Vt4.

4. A non-volatile semiconductor memory device comprising:

a memory cell array having a plurality of non-volatile memory cells each having four or more threshold voltage levels;

word lines, bit lines and source lines connected to said memory cells;

a row decoder configured to select one of said word lines; and

a column decoder configured to select one of said bit lines,

wherein when said four threshold voltage levels are given by Vt1, Vt2, Vt3 and Vt4 (Vt1<Vt2<Vt3<Vt4), respectively, the following steps (1) to (5) are executed to carry out a program operation,

(1) loading program data,

(2) programming for said memory cells to be given by the threshold voltage Vt4 being accomplished by a value which is equal to or higher than a maximum value of a program gate

voltage of said memory cells to be given by one of the threshold voltages Vt2 and Vt3,

(3) detecting whether the threshold voltage of said memory cells to be given by the threshold voltage Vt4 have the threshold voltage Vt4, and re-executing said step (2) when said memory cells do not have the threshold voltage Vt4, followed by a next step (4) when said memory cells have the threshold voltage Vt4,

(4) programming for said memory cells to be given by the threshold voltages Vt2 and Vt3 being carried out by said first gate voltage, and

(5) detecting whether said memory cells given by the threshold voltages Vt2 and Vt3 have said threshold voltages of Vt2 and Vt3, respectively, and re-executing said step (2) when said memory cells do not have the threshold voltages Vt2 and Vt3, respectively, while finishing said program operation when said memory cells have the threshold voltages Vt2 and Vt3.